

## 4-level capacitor-clamped boost converter with hard-switching and soft-switching implementations

A. N. Kasiran, A. Ponniran, A. A. Bakar, M. H. Yatim

Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Malaysia

---

### Article Info

#### Article history:

Received Mar 2, 2018

Revised Jul 9, 2018

Accepted Aug 24, 2018

---

#### Keywords:

Capacitor-clamped

Chopper

Hard-switching technique

Multilevel converter

Passive lossless snubber

Soft-switching technique

---

### ABSTRACT

This paper presents parameters analysis of 4-level capacitor-clamped boost converter with hard-switching and soft-switching implementation. Principally, by considering the selected circuit structure of the 4-level capacitor-clamped boost converter and appropriate pulse width modulation (PWM) switching strategy, the overall converter volume able to be reduced. Specifically, phase-shifted of  $120^\circ$  of each switching signal is applied in the 4-level capacitor-clamped boost converter in order to increase the inductor current ripple frequency, thus the charging and discharging times of the inductor is reduced. Besides, volume of converters is greatly reduced if very high switching frequency is considered. However, it causes increasing of semiconductor losses and consequently the converter efficiency is affected. The results show that the efficiency of 2-level conventional boost converter and 4-level capacitor-clamped boost converter are 98.59% and 97.67%, respectively in hard-switching technique, and 99.31% and 98.15%, respectively in soft-switching technique. Therefore, by applying soft-switching technique, switching loss of the semiconductor devices is greatly minimized although high switching frequency is applied. In this study, passive lossless snubber circuit is selected for the soft-switching implementation in the 4-level capacitor-clamped boost converter. Based on the simulation results, the switching loss is approximately eliminated by applying soft-switching technique compared to the hard-switching technique implementation.

Copyright © 2019 Institute of Advanced Engineering and Science.

All rights reserved.

---

### Corresponding Author:

Asmarashid Ponniran (A. Ponniran),  
Faculty of Electrical and Electronic Engineering,  
Universiti Tun Hussein Onn Malaysia,  
86400 Parit Raja, Johor, Malaysia.  
Email: asmar@uthm.edu.my

---

## 1. INTRODUCTION

Nowadays, transportation has become one of the most important thing to move from one place to another. However, due to the large number of automobile in a big city around the world, it has become the most critical issues which arise a pollution problem and may affect the environment and also to the human life [1]. To overcome this problem, the world today is approaching to the green transportation for example like electric vehicles. Due to the high voltage of the DC-link (200 V-400 V) [2]-[4], it difficult for the designer of electric vehicle system to integrate the power storage with the electric traction part. Thus, the system needs a power converter as an interface which has capability to handle the energy transfer from 12-48 V DC bus to the high voltage DC-link. DC-DC boost converters become the main key blocks inside the electric vehicle system as the auxiliary power supply of the electric load [5], [6]. Due to limitation space and weight in electric vehicle system, the optimization design of DC-DC boost converter is required [7]-[9]. Multilevel capacitor-clamped boost converter topology might be the attractive option in order to achieve high power density converter with considering high switching frequency. Besides that, due to the reduction of

voltage stress on semiconductor devices in multilevel capacitor-clamped boost converter, low rating of semiconductor devices can be used where it may reduce the conduction loss and switching loss.

Generally, hard-switching technique in PWM converters was used due to simple controls. The utilization of high switching frequency in DC-DC converter brings several advantages to the power converter e.g. low volume passive component, low  $dv/dt$  and  $di/dt$ . However, high switching frequency causes greater switching loss in the converter [10], [11]. This is due to the overlapping of current and voltage in semiconductor devices. Thus, in order to reduce the switching loss in converters circuit, soft-switching technique might be applied [12]-[15]. Passive lossless snubber is the effective technique for the soft-switching implementation in order to tackle this issue due to simple circuit structure to be considered.

This paper focuses on 4-level capacitor-clamped boost converter by applying two switching techniques, i.e., hard switching and soft switching, in order to observe the performance of the converters in term of efficiency. The discussion on both switching techniques are highlighted in this paper. The comparison of 4-level capacitor-clamped boost converter and 2-level conventional boost converter is discussed as well. Furthermore, the parameters design of 4-level capacitor-clamped boost converter is discussed. The switching loss and conduction loss of semiconductor devices are analyzed in order to observe the efficiency of converter. Simulation results are obtained in order to verify the realization of soft-switching at 4-level capacitor-clamped boost converter.

## 2. PARAMETERS DESIGN OF CONVERTER

Table 1 shows several parameters for designing conventional 2-level boost converter and 4-level capacitor-clamped boost converter. The current ripple and the voltage ripple are considered in order to appropriately select the inductor and capacitor, respectively [18]-[20]. By appropriately design the current ripple and voltage ripple, the size and volume of passive components is reduced, consequently the overall volume of the converter is reduced as well.

Table 1. Parameters design of converter

Parameter	Expressions	
Boost ratio, $\beta$	$\beta = \frac{1}{1-D}$	(1)
Output voltage, $V_{out}$ (V)	$V_{out} = \frac{V_{in}}{1-D}$	(2)
Boost inductor, $L_{(2-level)}$ (H)	$L_{(2-level)} = \frac{DV_{out}}{2f_{sw}\Delta I_{L(2-level)}}$	(3)
Boost inductor, $L_{(4-level)}$ (H)	$L_{(4-level)} = \frac{DV_{out}}{6f_{sw}\Delta I_{L(4-level)}}$	(4)
Capacitor-clamped 1, $C_1$ (F)	$C_{1(4-level)} = \frac{DI_{in}}{f_{sw}\Delta V_{C1}}$	(5)
Capacitor-clamped 2, $C_2$ (F)	$C_{2(4-level)} = \frac{DI_{in}}{f_{sw}\Delta V_{C2}}$	(6)
Output capacitor, $C_{out}$ (F)	$C_{out} = \frac{DP_{out}}{f_{sw}V_{out}\Delta V_{Cout(4-level)}}$	(7)

## 3. PRINCIPLE OF HARD-SWITCHING TECHNIQUE

Basically, DC-DC boost converter used PWM technique to control the turn-ON and turn-OFF of semiconductor devices in the power converter circuit. Figure 1(a) shows the circuit structure of 2-level conventional boost converter, meanwhile Figure 1(b) shows the circuit structure of 4-level capacitor-clamped boost converter. In the 4-level capacitor-clamped boost converter circuit configuration, it consists of three semiconductor switches  $S_1$ ,  $S_2$  and  $S_3$ . Meanwhile, for the operation mode, it requires 120-degree phase-shifted of the switching pattern to operate. Figure 2 shows the 120-degree phase shift PWM technique to control the turn-ON and turn-OFF of the semiconductor switches in the 4-level capacitor-clamped boost converter circuit.

Six operation modes in one full complete cycle, i.e., Mode 1 ( $S_2$  and  $S_3$  are turn-ON), Mode 2 (only  $S_3$  is turn-ON), Mode 3 ( $S_1$  and  $S_3$  are turn-ON), Mode 4 (only  $S_1$  is turn-ON), Mode 5 ( $S_1$  and  $S_2$  are turn-ON) and Mode 6 (only  $S_2$  is turn-ON). The unique feature in 4-level capacitor-clamped boost converter

circuit structure is the existing of middle capacitor which it shared the boost-up energy with the boost inductor where the inductor can be design smaller [20], [21].

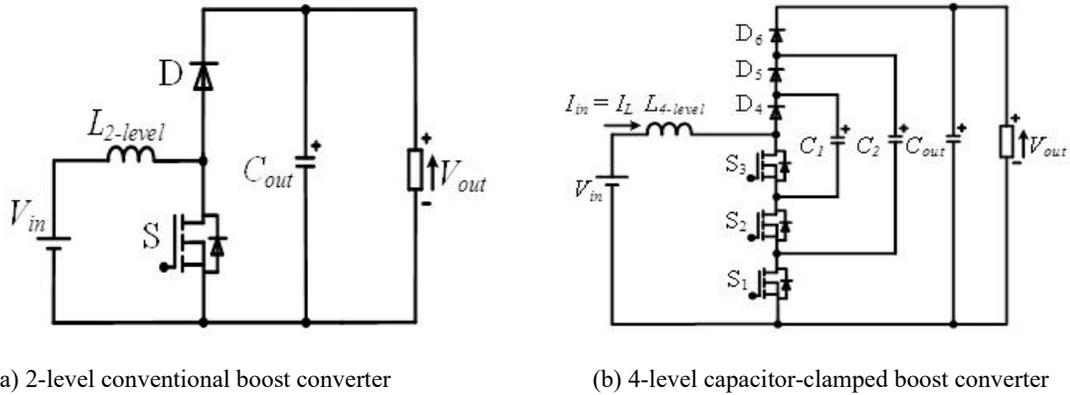


Figure 1. Circuit structure

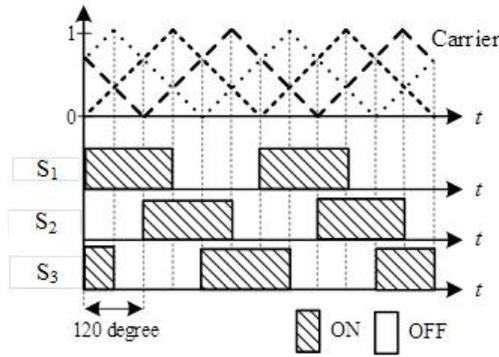


Figure 2. 120-degree phase-shifted PWM switching patterns

**3.1. Switching loss**

Basically, the switching loss in hard-switching technique occurred in two conditions which is during turn-ON and turn-OFF of the semiconductor devices. The switching loss is occurred due to the overlapping of current and voltage in switching devices as shown in Figure 3.

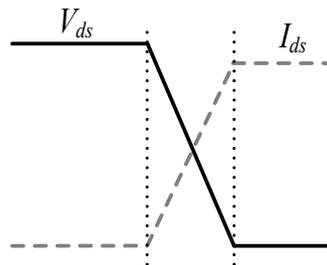


Figure 3. Illustration overlapping of current and voltage in switching devices

In hard-switching technique, the switching loss is estimated by considering the voltage ( $V_{ds}$ ) and current ( $I_{ds}$ ) of switching devices during operation. The summation of rise time ( $t_r$ ) and fall time ( $t_f$ ) of current

and voltage in switching devices are also taken into consideration. The switching loss of converter is determined in one switching period; thus, it requires switching frequency used for the converter as expressed in (8). The expression of the switching loss is expressed as follows:

$$P_{sw} = \left[ \frac{(I_{ds} V_{ds}) \times (t_r + t_f)}{6} \right] (f_{sw}) \tag{8}$$

**3.2. Conduction loss**

Theoretically, high conduction loss occurs due to large ON-resistance in switching devices. In multilevel structure, low rating of switching device can be selected due to low voltage stress on switching device. Thus, it reduces the conduction loss due to the small ON-resistance ( $R_{ON}$ ). Meanwhile, the conduction loss of diode is depending on forward rms current  $I_{f(rms)}$  where it considered maximum and minimum current of diode. Forward bias voltage ( $V_f$ ) is referred to the datasheet and  $D$  is the duty cycle used in the converter. The conduction loss for a switching device and a diode are expressed as follow:

$$P_{cond(m)} = I_{ds}^2 \times R_{ON} \times D \tag{9}$$

$$P_{cond(d)} = I_{F(rms)} \times V_f \tag{10}$$

**4. PRINCIPLE OF SOFT-SWITCHING TECHNIQUE**

Generally, there are several techniques in soft-switching i.e., active snubbers, resistor capacitor and diode (RCD) snubbers, resonant converter and passive lossless snubber. Active snubber circuit able to increase high efficiency of converter, but it requires additional circuits. Meanwhile, RCD snubbers have the worst performance even the circuit is simple due to the existing of resistor element [22]. However, passive lossless snubber has a simple circuit and able to increase the efficiency of converter. Due to this reason, passive lossless snubber is selected over the resonant converter due to the cost and reliability of the circuit. Figure 4 shows the three cells of passive lossless snubber circuit are added to the 4-level capacitor-clamped boost converter. Passive lossless snubber circuit consist of snubber inductors ( $L_{r1}, L_{r2}, L_{r3}$ ), snubber capacitors ( $C_{r1}, C_{r2}, C_{r3}$ ), buffer capacitors ( $C_{s1}, C_{s2}, C_{s3}$ ), and diodes ( $D_{s11}, D_{s12}, D_{s13}, D_{s21}, D_{s22}, D_{s23}, D_{s31}, D_{s32}, D_{s33}$ ).

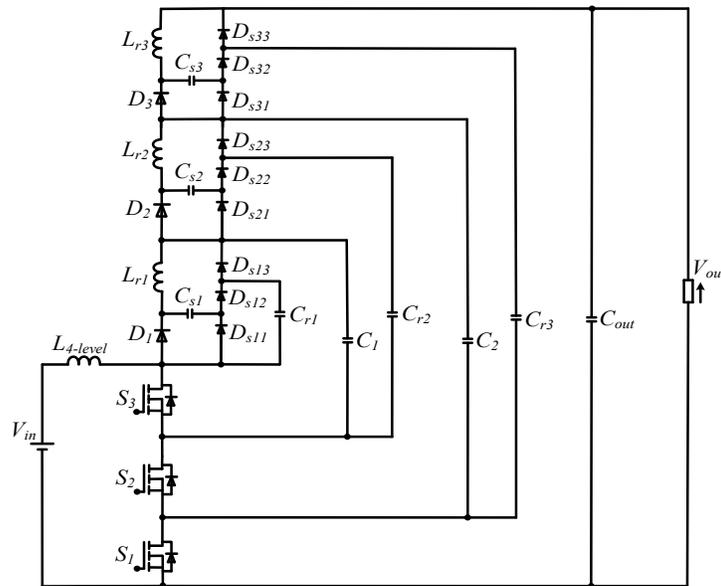


Figure 4. 4-level capacitor-clamped boost converter with passive lossless snubber circuit

Basically, switching loss is occurred due to the surge current in semiconductor devices. The passive lossless snubber circuit consist of snubber inductor and snubber capacitor that operated in order reduce the switching loss during turn-ON and turn-OFF of semiconductor devices. In other word, the snubber inductors and capacitors are added in order to realize the soft-switching conditions. Meanwhile, the buffer capacitor function as a tank of resonant energy for one complete cycle where the energy will transfer to the output. This is because the snubber circuit causes degradation of the output voltage. Thus, the buffer capacitor is added to realize the lossless snubber circuit operation. Principally, there is no power dissipated or accumulated in the snubber circuit components.

#### 4.1. Design guideline of passive lossless snubber circuit

In order to identify the value of snubber circuit of 4-level capacitor-clamped boost converter, several parameters are required to obtain. The value of snubber inductor, snubber capacitor and buffer capacitor were same for the three cells. Principally, the value of snubber inductor and snubber capacitor must be combined in a one resonant frequency where it can be expressed as follows:

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (11)$$

Then, the current range ( $I_{min}$  and  $I_{max}$ ) of switching device must be obtained to ensure the soft-switching can be achieved. The minimum and maximum current of switching device can be expressed as follows:

$$I_{min} = \frac{P_{in}}{V_{in-max}} \quad (12)$$

$$I_{max} = \frac{P_{in}}{V_{in-min}} \quad (13)$$

where the maximum current of switching device occurs during the input voltage in its minimum. Next, the range of duty cycle ( $D_{min}$  and  $D_{max}$ ) is calculate to ensure the minimum and maximum duty cycle where the soft-switching occur. The minimum and maximum duty cycle can be expressed as follows:

$$D_{min} = 1 - \frac{V_{in-max}}{V_{out}} \quad (14)$$

$$D_{max} = 1 - \frac{V_{in-min}}{V_{out}} \quad (15)$$

where the minimum duty cycle occurs when the input voltage in its maximum. By relating the inductance and capacitance snubbers with the resonant interval times where it can be suggested less than some fraction ( $0 < k < 1$ ) of the switching period  $T_s$ . Thus, this relation can be expressed as follows:

$$\frac{2\pi}{\omega_r} \leq kT_s \quad (16)$$

where the appropriate value of  $k$  is selected for a required  $Tr_{-on}$  or  $Tr_{-off}$ . The value of  $k$  is select by refer to the Figure 5 where the smallest value of  $k$  is selected and which satisfies the largest allowable value of  $Tr_{-on}$  and  $Tr_{-off}$ . From Figure 5, IR is the current ratio of maximum current and minimum current. Meanwhile,  $x$  is the ratio of snubber capacitor and buffer capacitor which can be equate by 0.1. The detail of design principle is given in the paper [12], [13]. The interval for  $Tr_{-on}$  is  $I = I_{max}$  where it represents the worst case, meanwhile for  $Tr_{-off}$  interval, several current ratios are shown in Figure 5.

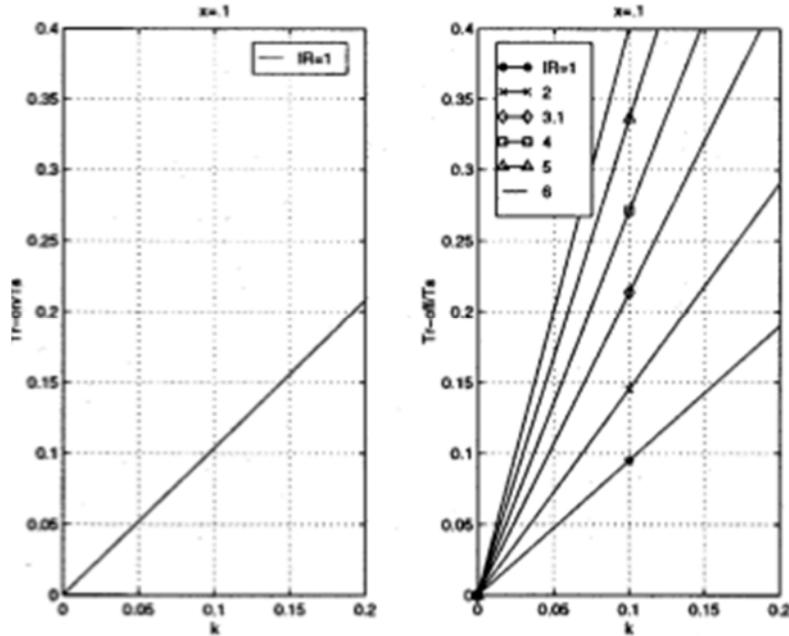


Figure 5. The intervals of resonant turn-ON and resonant turn-OFF [12]

After several parameters has been determined, the value of snubber inductor, snubber capacitor, and buffer capacitor can be calculated by using the expressions as follows:

$$L_r = \frac{kT_s V_{out}}{2\pi I_{max}} \tag{17}$$

$$C_r = \frac{kT_s I_{max}}{2\pi V_{out}} \tag{18}$$

$$C_s = \frac{C_r}{0.1} \tag{19}$$

**4.2. Switching loss reduction**

Principally, passive lossless snubber circuit are added in order to eliminate or reduce the switching loss in 4-level capacitor-clamped boost converter. The function of snubber inductor and snubber capacitor in passive lossless snubber circuit are to prevent the overlapping between current and voltage in semiconductor devices during turn-ON and turn-OFF conditions where the voltage across the semiconductor devices is reduced to zero before the current rises. Figure 6 shows the illustration of soft-switching during turn-ON of switching device

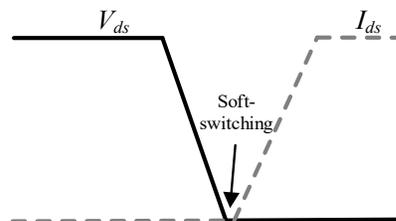


Figure 6. Illustration of soft-switching during turn-ON condition

By applying passive lossless snubber circuit, the switching loss in 4-level capacitor-clamped boost converter is approximately eliminated where the switching loss are approximately zero. Thus, the switching loss in 4-level capacitor-clamped boost converter can be neglected in order to calculate the efficiency of the converter. In 4-level capacitor-clamped boost converter only consider conduction loss of semiconductor devices which MOSFETs and diodes.

#### 4.3. Balancing of voltage stress on switching devices

In order to achieve soft-switching condition, the voltage stress on switching devices must be balanced. Thus, maximum and minimum voltage and current of switching devices can be determined. Due to improper charging and discharging of capacitors in 4-level capacitor-clamped boost converter, automatic voltage regulator controller is required to control the charging and discharging of capacitor-clamped [8]. Failure to balance the capacitor-clamped voltage, may causes the voltage stress on switching devices unbalanced. However, this paper only considers natural balancing circuit in order to balance the voltage stress on switching devices in 4-level capacitor-clamped boost converter circuit.

Basically, natural balancing circuit only consists of inductor and capacitor. In order to determine the inductance and capacitance of natural balancing circuit, the parameters are complement each other. However, due to multilevel structure, the resonant frequency is equal to three times of switching frequency. The natural balancing circuit is connected at the input side of 4-level capacitor-clamped boost converter circuit which is parallel with the three switching devices. Commonly, the inductance and capacitance of natural balancing circuit used are small in value. Even though, the natural balancing circuit is used, for a better results and performance of converter, closed loop controller is recommended in order to control the charging and discharging of capacitor-clamped which can affect the voltage stress on switching devices in multilevel structure circuit.

## 5. SIMULATION RESULTS

Table 2 shows the specifications of 2-level conventional boost converter and 4-level capacitor-clamped boost converter by using hard-switching technique. Meanwhile, Table 3 shows the selected specifications of soft-switching circuit for 2-level conventional boost converter and 4-level capacitor-clamped boost converter.

Table 2. Specifications for hard-switching technique

Specifications	Value
Output power, $P_{out}$ (W)	1600
Output voltage, $V_{out}$ (V)	400
Duty cycle, $D$	0.5
Switching frequency, $f_{sw}$ (kHz)	15, 30, 50
Boost inductor, $L_{(2-level)}$ (mH)	0.5
Boost inductor, $L_{(4-level)}$ (mH)	0.5
Capacitor-clamped 1, $C_1$ ( $\mu$ F)	200
Capacitor-clamped 2, $C_2$ ( $\mu$ F)	200
Output capacitor, $C_{out}$ ( $\mu$ F)	470

Table 3. Selected specifications of soft-switching circuit

Parameter	Value		
Switching frequency, $f_{sw}$ (kHz)	15	30	50
Snubber inductor, $L_r$ ( $\mu$ H)	8	4	2
Snubber capacitor, $C_r$ (nF)	10	5	3
Buffer capacitor, $C_b$ ( $\mu$ F)	100	50	30

#### 5.1. Losses analysis in hard-switching technique

In this analysis, same specifications are used for 2-level conventional boost converter and 4-level capacitor boost converter by using selected switching frequency which are 15 kHz, 30 kHz, and 50 kHz. Principally, in hard-switching technique, the switching loss is increased when high switching frequency is used. IXFH20N80Q of MOSFET model and VS-20ETSPBF of diode model are considered for analysis of 2-level conventional boost converter. Meanwhile, NTE2921 of MOSFET model and SBR20A300CT of diode model are considered for 4-level capacitor-clamped boost converter. Thus, from the simulation results, it has been verified that the switching loss is increased as the high switching frequency is used. However, the

conduction loss remains same. This is because the conduction loss is not related to the switching period. In order to obtain the efficiency of the converters, the losses only consider switching loss and conduction loss of semiconductor devices. Table 4 shows the losses analysis of 2-level conventional boost converter and 4-level capacitor-clamped boost converter in hard-switching technique with different switching frequencies. The total power losses consist of switching loss at MOSFET and conduction loss at MOSFET and diode. By considering the switching frequency 50 kHz, the total power losses increase in 2-level conventional boost converter and 4-level capacitor-clamped boost converter where the value is 22.53 W and 37.31 W, respectively. Almost 30% switching loss increases by increasing the switching frequency to 30 kHz. Meanwhile, almost 70% switching loss increases by increasing the switching frequency to 50 kHz. The efficiency for 2-level conventional boost converter and 4-level capacitor-clamped boost converter is 98.59% and 97.67%, respectively. Due to an additional of semiconductor devices, the total power losses increase in 4-level capacitor-clamped boost converter. In this analysis, the losses of 2-level conventional boost converter have the lower value if compared to the 4-level capacitor-clamped boost converter as high switching frequency is used. Figure 7 shows the total power losses of 2-level conventional boost converter and 4-level capacitor-clamped boost converter against switching frequency. Meanwhile, Figure 8 shows the simulation result of 2-level conventional boost converter and 4-level capacitor-clamped boost converter in hard-switching condition with switching frequency 15 kHz is used.

**Table 4. Losses when using Hard-switching Technique**

Converter Structure	Switching Frequency ( $f_{sw}$ )	Switching Loss ( $P_{sw}$ )	Conduction Loss ( $P_{cond}$ )	Total Power Losses ( $P_{loss}$ )
2-level conventional boost converter	15 kHz	0.33 W	21.44 W	21.77 W
	30 kHz	0.66 W	21.44 W	22.10 W
	50 kHz	1.09 W	21.44 W	22.53 W
4-level capacitor-clamped boost converter	15 kHz	0.58 W	26.88 W	35.94 W
	30 kHz	1.17 W	26.88 W	36.53 W
	50 kHz	1.95 W	26.88 W	37.31 W

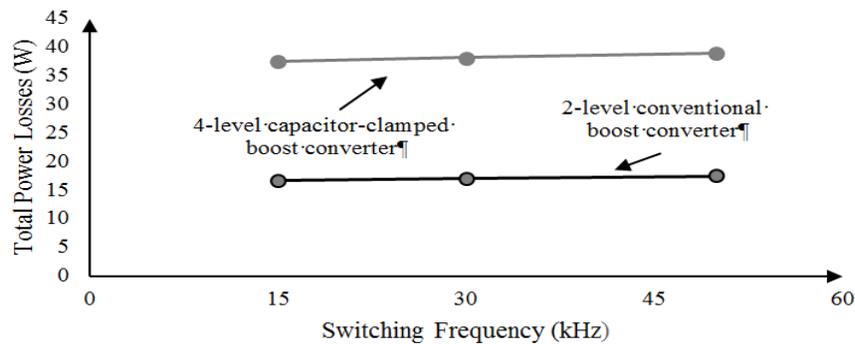


Figure 7. Graph of total power losses against switching frequency

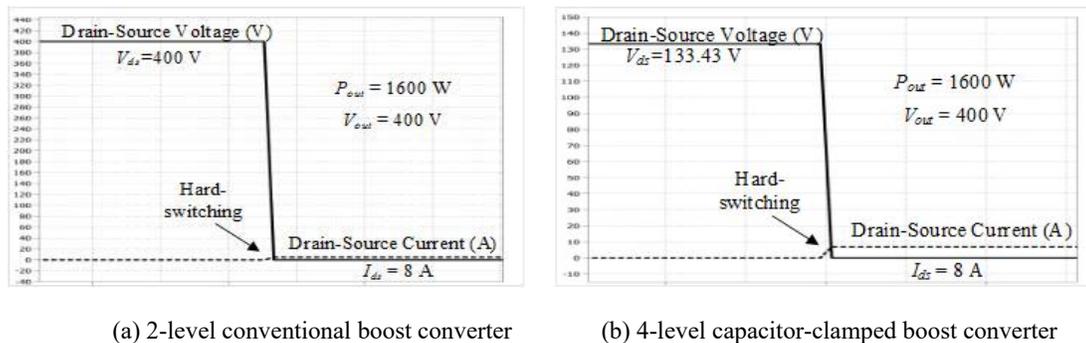


Figure 8. Simulation result in hard-switching condition with  $f_{sw}=15$  kHz

**5.2. Power losses reduction in soft-switching technique**

In order to analyze this part, the parameter selection of passive lossless snubber circuit in Table 3 are considered. From the simulation results, it shows that the passive lossless snubber circuit are able to tackle the problem of switching loss in 2-level conventional boost converter and 4-level capacitor-clamped boost converter. Basically, this passive lossless snubber circuit realizes soft-switching condition during turn-ON and turn-OFF of the semiconductor devices. The simulation result shows that the switching loss of semiconductor devices in both converters is approximately zero. Figure 9 shows the soft-switching conditions of 2-level conventional boost converter and 4-level capacitor-clamped boost converter is achieved during the turn-ON condition at  $S_1$ . From the results, there are no overlapping between current and voltage in semiconductor devices which lead to no switching loss produced. Table 5 shows the losses analysis of 2-level conventional boost converter and 4-level capacitor-clamped boost converter which only consider conduction loss of MOSFET and diode due to switching loss is too small and can be neglected. Meanwhile, Figure 10 shows the graph of total power losses against switching frequency for 2-level conventional boost converter and 4-level capacitor-clamped boost converter.

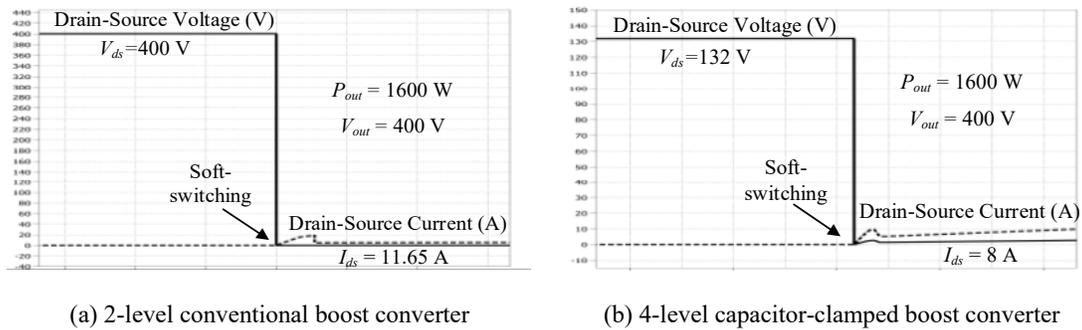


Figure 9. Simulation result of soft-switching condition with  $f_{sw} = 15 \text{ kHz}$

Table 5. Losses When Using Soft-Switching Technique

Converter Structure	Switching Frequency ( $f_{sw}$ )	Switching Loss ( $P_{sw}$ )	Conduction Losses ( $P_{cond}$ )	Total Power Losses ( $P_{loss}$ )
2-level conventional boost converter	15 kHz	Approximately equal to 0 W	12.25 W	12.25 W
	30 kHz	(Neglected)	11.38 W	11.38 W
	50 kHz	(Neglected)	11.05 W	11.05 W
4-level capacitor-clamped boost converter	15 kHz	Approximately equal to 0 W	28.15 W	28.15 W
	30kHz	(Neglected)	29.47 W	29.47 W
	50 kHz	(Neglected)	29.67 W	29.67 W

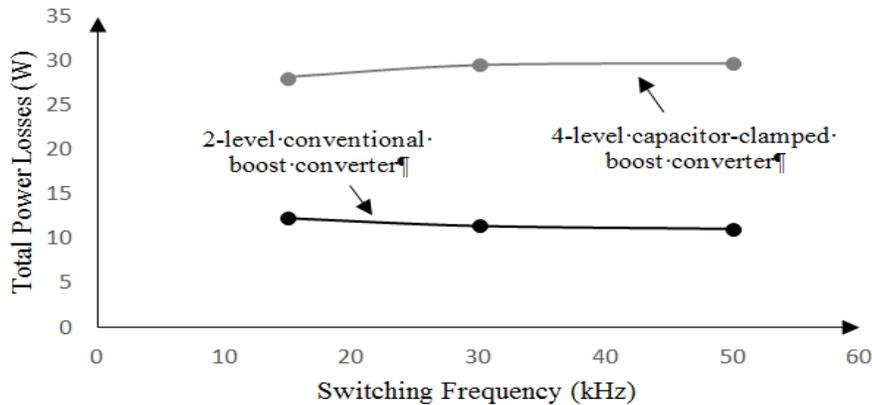


Figure 10. Graph of total power losses against switching frequency

The total power losses in 2-level conventional boost converter and 4-level capacitor-clamped boost converter is reduced if compared to the hard-switching technique. Even though high switching frequency is used, the total power losses of converters by using passive lossless snubber circuit is lower than the converters using hard-switching technique. From the result, total power losses in 2-level conventional boost converter and 4-level capacitor-clamped boost converter in 50 kHz switching frequency are 11.05 W and 29.67 W, respectively. If the losses result is compared with hard-switching technique, the losses in soft-switching technique is reduced. The efficiency of 2-level conventional boost converter and 4-level capacitor-clamped boost converter increase by using soft-switching technique, where the efficiency is 99.31% and 98.15%, respectively. By increasing the switching frequency, the time-ON for the semiconductor devices become smaller which cause the conduction loss decrease. Thus, soft-switching technique plays a vital role in order to reduce the switching loss of semiconductor devices, where this technique is more effective when high switching frequency is used.

## 5. CONCLUSION

As the conclusion, the authors have discussed and compared the efficiency of 2-level conventional boost converter and 4-level capacitor-clamped boost converter by applying hard-switching technique and soft-switching techniques. The losses at semiconductor devices, which are switching loss and conduction loss, are considered. In simulation works, the switching loss issue is rectified by applying soft-switching, where it has been realized by using passive lossless snubber circuit. The additional circuit of soft-switching may reduce the losses of converter at high switching frequency. Due to high switching frequency, the volume of converter can be reduced as well. Moreover, the circuit structure of 4-level capacitor-clamped boost converter also able to reduce the converter volume. Furthermore, by applying soft-switching technique, the range of duty cycle for a converter is limited. Figure 11 shows the relationship between volume of converter and losses of converter by using hard-switching or soft-switching techniques when high switching frequency is considered.

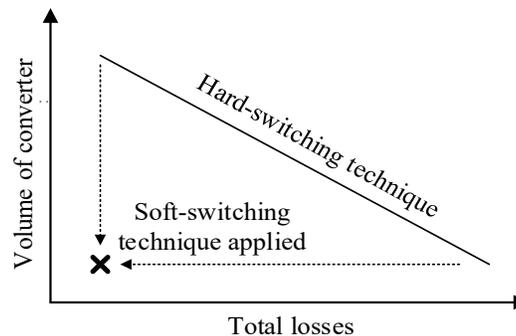


Figure 11. Relationship of volume converter and total losses by using different switching techniques

## ACKNOWLEDGEMENT

The authors would like to express their appreciation to the Universiti Tun Hussein Onn Malaysia. This research is funded by the Universiti Tun Hussein Onn Malaysia under Tier 1 Research Grant (Vot No. U858) and GPPS Research Grant (Vot No. U951).

## REFERENCES

- [1] M. Al Sakka, J. Van Mierlo, and H. Gualous, "DC/DC Converters for Electric Vehicles," S. B. T.-E. V.-M. and S. Soyly, Ed. Rijeka: InTech, p. Ch. 13, 2011.
- [2] A. Ponniran, K. Orikawa, and J. Itoh, "Fundamental Operation of Marx Topology for High Boost Ratio DC-DC Converter," *IEEJ J. Ind. Appl.*, vol. 5, no. 4, pp. 329–338, 2016.
- [3] A. B. Ponniran, K. Orikawa, and J. i. Itoh, "Interleaved high boost ratio Marx topology DC-DC converter," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, pp. 1–6, 2015.

- [4] A. Ponniran, K. Orikawa, and J. I. Itoh, "Modular multi-stage Marx topology for high boost ratio DC/DC converter in HVDC," in *INTELEC, International Telecommunications Energy Conference (Proceedings)*, vol. 2016–Septe, pp. 1–6, 2016.
- [5] B. S. Kim, H. J. Kim, C. Jin, and D. Y. Huh, "A digital controlled DC-DC converter for electric vehicle applications," in *2011 International Conference on Electrical Machines and Systems*, 2011, pp. 1–5.
- [6] W. H. Martinez and C. A. Cortes, "High power density interleaved DC-DC converter for a high performance electric vehicle," in *2013 Workshop on Power Electronics and Power Quality Applications (PEPQA)*, pp. 1–6, 2013.
- [7] A. A. Bakar, M. U. Wahyu, A. Ponniran, and T. Taufik, "Simulation and Analysis of Multiphase Boost Converter with Soft-Switching for Renewable Energy Application," *Int. J. Power Electron. Drive Syst. (JPEDS)*; Vol 8, No 4 December 2017, Nov. 2017.
- [8] M. A. Harimon, A. Ponniran, A. N. Kasiran, and H. H. Hamzah, "A study on 3-phase interleaved DC-DC boost converter structure and operation for input current stress reduction," *Int. J. Power Electron. Drive Syst.*, vol. 8, no. 4, pp. 1948–1953, 2017.
- [9] W. Martinez, S. Kimura, J. Imaoka, M. Yamamoto, and C. A. Cortes, "Volume comparison of DC-DC converters for electric vehicles," in *2015 IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA)*, pp. 1–6, 2015.
- [10] G. V. I. T. U. Ganesan R and M. . V. I. T. U. Prabhakar, "Multi-Level DCDC Converter for High Gain Applications," *International Journal of Power Electronics and Drive System (JPEDS)*, vol. 3, no. 4, pp. 365–373, 2013.
- [11] J. Y. Zhu and D. H. Ding, "Zero voltage and zero current switched PWM DC-DC converters using active snubber technique," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, vol. 2, pp. 1574–1579 vol.2, 1998.
- [12] J. Y. Zhu and D. H. Ding, "Zero voltage and zero current switched PWM DC-DC converters using active snubber technique," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, 1998, vol. 2, pp. 1574–1579 vol.2.
- [13] R. I. U. Sharma Ahmedabad, India, "Soft Switched Multi-Output PWM DC-DC Converter," *Int. J. Power Electron. Drive Syst.*, vol. 3, no. 3, pp. 328–335, 2013.
- [14] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, 1995.
- [15] K. V. R. Kishore, B. F. Wang, K. N. Kumar, and P. L. So, "A new ZVS full-bridge DC-DC converter for battery charging with reduced losses over full-load range," in *2015 Annual IEEE India Conference (INDICON)*, pp. 1–6, 2015.
- [16] G. Hua and F. C. Lee, "Soft-switching techniques in (PWM) converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, 1995.
- [17] V. R. K. Kanamarlapudi, B. Wang, N. K. Kandasamy, and P. L. So, "A New ZVS Full-Bridge DC-DC Converter for Battery Charging with Reduced Losses over Full-Load Range," *IEEE Trans. Ind. Appl.*, vol. 9994, no. c, pp. 1–1, 2017.
- [18] A. Bin Ponniran, K. Orikawa, and J. Itoh, "Minimum Flying Capacitor for N-Level Capacitor DC/DC Boost Converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3255–3266, 2016.
- [19] A. N. Kasiran and A. Ponniran and M. A. Harimon and H. H. Hamzah, "A Study of 4-level DC-DC Boost Inverter with Passive Component Reduction Consideration," *J. Phys. Conf. Ser.*, vol. 995, no. 1, p. 12062, 2018.
- [20] A. Bin Ponniran, K. Matsuura, Koji Orikawa, and J. Itoh, "Size Reduction of DC-DC Converter using Flying Capacitor Topology with Small Capacitance," *IEEE J. Ind. Appl.*, vol. 3, no. 6, pp. 446–454, 2014.
- [21] A. Ponniran *et al.*, "Volume reduction consideration in multilevel DC-DC boost converter," in *4th IET Clean Energy and Technology Conference*, p. 2 (5 .)-2 (5 .), 2016.
- [22] C.-J. Tseng and C.-L. Chen, "A passive lossless snubber cell for nonisolated PWM DC/DC converters," *IEEE Trans. Ind. Electron.*, vol. 45, no. 4, pp. 593–601, 1998.
- [23] K. M. Smith and K. M. Smedley, "Engineering design of lossless passive soft switching methods for PWM converters. I. With minimum voltage stress circuit cells," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 336–344, 2001.
- [24] K. M. Smith and K. M. Smedley, "Engineering design of lossless passive soft switching methods for PWM converters. II. With nonminimum voltage stress circuit cells," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 864–873, 2002.

**BIOGRAPHIES OF AUTHORS**

Mohd Amirul Naim Bin Kasiran received the bachelor's degree in Electrical Engineering (Power) from Universiti Tun Hussein Onn Malaysia, Parit Raja, Malaysia, in 2017. He is currently working toward master's in electrical engineering also at Universiti Tun Hussein Onn Malaysia.



Asmarashid Bin Ponniran received the bachelor's degree in electrical engineering from Universiti Tun Hussein Onn Malaysia, Parit Raja, Malaysia, in 2002, and the master's degree in electrical engineering (power) from Universiti Teknologi Malaysia, Johor Bahru, Malaysia, in 2005. Then, he received the Ph.D degree in electrical engineering from the Nagaoka University of Technology, Nagaoka, Japan. He is currently working as lecturer with Universiti Tun Hussein Onn Malaysia. His research interest includes power converter, underground power cable in distribution side, and demand side management of power consumption.



Afarulrazi Bin Abu Bakar was born in Johor, Malaysia on May 18, 1980. He received his M.Eng. (Electrical) from University Tun Hussein Onn Malaysia (UTHM) in 2007 and B.Eng. (Electrical) from University Teknologi Mara (UiTM) in 2004. He has been working as a lecturer in Department of Electrical Power Engineering, Faculty of Electrical and Electronic Engineering, UTHM since 2007. Currently he is persuing Ph.D degree in UTHM. His research interests include the area of power electronics and renewable energy.



Mohd Hafizie Bin Yatim received the bachelor's degree in electrical engineering technology from Universiti Tun Hussein Onn Malaysia, Parit Raja, Malaysia, in 2017. He is currently working toward master's in electrical engineering also at Universiti Tun Hussein Onn Malaysia.